What is claimed is:

1. A method of fabricating a semiconductor device comprising:

forming first type well regions within a core logic portion and an embedded memory portion of the device;

forming second type well regions within the core logic portion and the embedded memory portion of the device;

performing a supplemental isolation implant within at least one of the first type well regions of the embedded memory portion to modify dopant profile(s) of the at least one of the first type well regions to increase isolation.

2. The method of claim 1, further comprising performing a supplemental isolation implant within at least one of the second type well regions to modify dopant profile(s) of the at least one of the second type well regions to increase isolation.

3. The method of claim 2, wherein the first type well regions are n-type and the second type well regions are p-type.

4. The method of claim 2, wherein the first type well regions are p-type and the second type regions are n-type.

5. The method of claim 1, further comprising forming first shallow trench isolation regions having a first width that separate active regions across well boundaries within the core logic portion and forming second shallow trench isolation regions having a second width that separate active regions across well boundaries within the embedded memory portion.

6. The method of claim 5, wherein the second width is less than the first width.

7. The method of claim 5, wherein the second width is substantially less than the first width.

8. The method of claim 1, further comprising forming stacked gate structures prior to performing a supplemental isolation implant.

9. The method of claim 1, wherein performing a supplemental isolation implant within the first type well regions of the embedded memory portion comprises:

forming a layer of resist on the device and selectively exposing the first type well regions of the embedded memory; and

implanting one or more dopants of the first type into the exposed first type well regions.

10. The method of claim 9, wherein the layer of resist formed is also employed to raise a threshold voltage of high-threshold-voltage transistors formed on the device.

11. The method of claim 10, wherein the threshold voltage of the high-threshold-voltage transistors is raised using a channel implant.

12. The method of claim 10, wherein the threshold voltage of the high-threshold-voltage transistors is raised using a pocket implant.

13. A method of fabricating a semiconductor device comprising:

forming a core logic portion and an embedded memory portion;

forming shallow trench isolation regions having a first width between active regions across well boundaries within the core logic portion;

forming shallow trench isolation regions having a second width between active regions across well boundaries within the embedded memory portion

forming n-well regions having a selected dopant profile within the core logic portion and the embedded memory portion

forming p-well regions having a selected dopant profile within the core logic portion and the embedded memory portion

adjusting the dopant profile of the n-well regions of the embedded memory portion to a n-well isolation dopant profile; and

adjusting the dopant profile of the p-well regions of the embedded memory portion to a p-well isolation dopant profile.

14. The method of claim 13, wherein the n-well isolation dopant profile is a function of the second width and a permitted junction capacitance for the embedded memory portion.

15. The method of claim 13, further comprising determining isolation requirements for the core logic portion and the embedded memory portion and selecting the first width and the second width according to the determined isolation requirements.

16. The method of claim 15, wherein the isolation requirements are related to junction capacitance requirements.

17. A method of fabricating a semiconductor device comprising:

selectively forming first type well regions within a core logic portion to a first depth;

selectively forming second type well regions within the core logic portion;

and an embedded memory portion of the device to a second depth;

selectively forming first type well regions within an embedded memory portion of the device to a third depth, wherein the third depth is less than the first depth; and

selectively forming second type well regions within the embedded memory portion of the device to a fourth depth, wherein the fourth depth is less than the second depth.

18. The method of claim 17, further comprising forming shallow trench isolation regions within the core logic portion and the embedded memory portion wherein the isolation regions formed in the embedded memory portion have relatively smaller isolation spacings.

19. The method of claim 18, wherein the fourth depth and the third depth of the embedded memory are less than a depth of the shallow trench isolation regions of the embedded memory.

20. The method of claim 17, further comprising biasing at least one of the first type well regions within the embedded memory under an active region with butted contact(s).

21. A method of fabricating a semiconductor device comprising:

forming first type well regions within a core logic portion having a selected dopant profile;

forming second type well regions within the core logic portion having a selected dopant profile, wherein the second type is opposite of the first type;

forming first type well regions within an embedded memory portion having a selected dopant profile that is distinct from the dopant profile of the first type well regions within the core logic portion; and

forming second type well regions within the embedded memory portion having a selected dopant profile that is distinct from the dopant profile of the second type well regions within the core logic portion.

22. The method of claim 21, wherein the embedded memory portion that the first type well regions and the second type well regions are formed in is static random-access memory.

23. The method of claim 21, wherein the dopant profile of the first type well regions within the embedded memory portion provides relatively increased isolation compared with the dopant profile of the first type well regions within the core region.

24. The method of claim 21, wherein forming the first type well regions within the embedded memory portion comprises performing a supplemental isolation implant within the first type well regions within the embedded memory portion to obtain the dopant profile of the first type well regions within the embedded memory portion.

25. The method of claim 24, wherein performing the isolation implant occurs during a threshold voltage adjustment implant.

26. A semiconductor device comprising:

a core logic comprising a plurality of PMOS transistors formed in n-wells and NMOS transistors formed in p-wells, wherein adjacent MOS transistors are separated across well boundaries by a shallow trench isolation region having a first width

an embedded memory array comprising a plurality of PMOS transistors formed in n-wells and NMOS transistors formed in p-wells, wherein adjacent

MOS transistors are separated are separated across well boundaries by a shallow trench isolation region having a second width that is less than the first width, and wherein dopant concentration of the n-wells and p-wells of the embedded memory are greater than a dopant concentration of the n-wells and p-wells of the core logic.

27. The semiconductor device of claim 18, wherein the dopant concentration of the n-wells in the core logic at a depth of 350 nm is $8x10^{17}$ cm^3 and the dopant concentration of the n-wells in the embedded memory array at a depth of 350 nm is $1.6x10^{18}$ cm^3.

28. The semiconductor device of claim 18, wherein the MOS transistors of the embedded memory array have a relatively higher junction capacitance than the MOS transistors of the core logic.